Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method of generating a set of test patterns ~~for one of simulating and testing a layout of an integrated circuit~~, the method which comprises the steps of:

(a) generating a set of test patterns on a random basis for one of simulating and testing a layout of an integrated circuit;

(b) applying the set of test patterns to ~~an~~ the integrated circuit by using an automatic test equipment;

(c) determining outputs of the integrated circuit;

(d) processing the outputs in order to determine whether given test criteria are met; and

(e) depending on a determination result in step (d), generating a new set of test patterns based on the set of test patterns generated in step (a) by using a genetic algorithm.

Claim 2 (original): The method according to claim 1, which comprises repeating steps (b) to (e) until the given test criteria are met.

Claim 3 (original): The method according to claim 1, which comprises:

(f) repeating steps (b) to (e) until a condition is met, the condition being selected from the group consisting of meeting the given test criteria and repeating steps (b) to (e) a given number of times.

Claim 4 (original): The method according to claim 3, which comprises:

generating a new set of test patterns on a random basis, if the given test criteria are not met after repeating steps (b) to (e) the given number of times; and

repeating step (f) based on the new set of test patterns.

Claim 5 (original): The method according to claim 1, which comprises concluding that the given test criteria are met if the set of test patterns is associated with an average fitness above a given value.

Claim 6 (original): The method according to claim 2, wherein step (e) includes combining at least some of the test patterns according to the genetic algorithm in order to generate the new set of test patterns.

Claim 7 (original): The method according to claim 6, which comprises:

selecting test patterns from the set of test patterns according to given selection criteria in order to provide selected test patterns; and

combining the selected test patterns according to the genetic algorithm in order to generate the new set of test patterns.

Claim 8 (original): The method according to claim 7, which comprises selecting a test pattern if the test pattern is associated with a fitness value greater than a reference value.

Claim 9 (original): The method according to claim 7, which comprises:

(g) selecting a test pattern if the test pattern is associated with a highest fitness value of all unselected test patterns.

Claim 10 (original): The method according to claim 9, which comprises repeating step (g) until a given percentage of test patterns has been selected.

Claim 11 (original): The method according to claim 9, wherein step (e) includes:

(h) sorting the selected test patterns according to an order of associated fitness values;

(i) randomly selecting parent test patterns from test patterns as sorted in step (h) in order to provide selected parent test patterns; and

(j) combining the selected parent test patterns.

Claim 12 (original): The method according to claim 1, which comprises using, as the genetic algorithm, an algorithm having at least one element selected from the group consisting of a crossing over, a re-combination, and a mutation of selected ones of the test patterns.

Claim 13 (original): The method according to claim 1, wherein step (a) includes generating a plurality of sets of test patterns, each set of test patterns being included in a test pattern population.

Claim 14 (original): The method according to claim 13, which comprises performing steps (a) to (e) for each respective test pattern population.

Claim 15 (currently amended): A method of generating a set of input signals ~~for one of simulating and testing a layout of an integrated circuit~~, the method which comprises the steps of:

(m) generating a plurality of sets of input signals for one of simulating and testing a layout of an integrated circuit;

(n) applying the plurality of sets of input signals to ~~an~~ the integrated circuit by using an automatic test equipment;

(o) determining outputs of the integrated circuit;

(p) processing the outputs in order to determine whether given test criteria are met; and

(q) depending on a determination result in step (p), generating a new plurality of sets of input signals based on the plurality of sets of input signals generated in step (m) by using a genetic algorithm.

Claim 16 (original): The method according to claim 15, which comprises generating the plurality of sets of input signals such that at least some of the input signals are associated with a number of AC/DC parameters.

Claim 17 (original): The method according to claim 15, which comprises providing respective given parameters of each respective one of the sets of input signals such that given parameters of each one of the sets of input signals varies from given parameters of each other one of the sets of input signals.

Claim 18 (original): The method according to claim 15, which comprises repeating steps (n) to (q) until the given test criteria are met.

Claim 19 (original): The method according to claim 15, which comprises:

(r) repeating steps (n) to (q) until a condition is met, the

condition being selected from the group consisting of meeting the given test criteria and repeating steps (n) to (q) a given number of times.

Claim 20 (original): The method according to claim 15, which comprises concluding that the given test criteria are met if the plurality of sets of input signals is associated with a worst case of operation situation.

Claim 21 (original): The method according to claim 15, wherein step (q) includes combining at least some of corresponding ones of the input signals of different sets of input signals according to the genetic algorithm in order to generate a new set of input signals.

Claim 22 (currently amended): A method of generating test patterns and input signals ~~for one of simulating and testing a layout of an integrated circuit~~, the method which comprises the steps of:

generating a set of test patterns on a random basis <u>for one of simulating and testing a layout of an integrated circuit</u>, applying the set of test patterns to ~~an~~ <u>the</u> integrated circuit by using an automatic test equipment and processing outputs of the integrated circuit in order to determine whether given

test criteria are met, and, depending on a determination result, generating a new set of test patterns based on the set of test patterns by using a genetic algorithm; and

generating a plurality of sets of input signals for one of simulating and testing the layout of the integrated circuit, applying the plurality of sets of input signals to the integrated circuit by using the automatic test equipment and processing outputs of the integrated circuit in order to determine whether given test criteria are met, and, depending on a determination result, generating a new plurality of sets of input signals based on the plurality of sets of input signals by using a genetic algorithm.

Claim 23 (original): A data processing configuration, comprising:

an automatic test equipment; and

a data processing system operatively connected to said automatic test equipment, said data processing system being programmed to generate a set of test patterns on a random basis, apply the set of test patterns to an integrated circuit by using said automatic test equipment, determine outputs of the integrated circuit, process the outputs in order to

determine whether given test criteria are met, and depending on a determination result, generate a new set of test patterns based on the set of test patterns by using a genetic algorithm.

Claim 24 (original): A data processing configuration, comprising:

an automatic test equipment; and

a data processing system operatively connected to said automatic test equipment, said data processing system being programmed to generate a plurality of sets of input signals, apply the plurality of sets of input signals to an integrated circuit by using said automatic test equipment, determine outputs of the integrated circuit, process the outputs in order to determine whether given test criteria are met, and depending on a determination result, generate a new plurality of sets of input signals based on the plurality of sets of input signals by using a genetic algorithm.

Claim 25 (currently amended): A computer-readable medium having computer-executable instructions for performing a method of generating a set of test patterns ~~for one of~~

~~simulating and testing a layout of an integrated circuit~~, the method which comprises the steps of:

(a) generating a set of test patterns on a random basis for one of simulating and testing a layout of an integrated circuit;

(b) applying the set of test patterns to ~~an~~ the integrated circuit by using an automatic test equipment;

(c) determining outputs of the integrated circuit;

(d) processing the outputs in order to determine whether given test criteria are met; and

(e) depending on a determination result in step (d), generating a new set of test patterns based on the set of test patterns generated in step (a) by using a genetic algorithm.

Claim 26 (currently amended): A computer-readable medium having computer-executable instructions for performing a method of generating a set of input signals ~~for one of simulating and testing a layout of an integrated circuit~~, the method which comprises the steps of:

(m) generating a plurality of sets of input signals for one of simulating and testing a layout of an integrated circuit;

(n) applying the plurality of sets of input signals to ~~an~~ the integrated circuit by using an automatic test equipment;

(o) determining outputs of the integrated circuit;

(p) processing the outputs in order to determine whether given test criteria are met; and

(q) depending on a determination result in step (p), generating a new plurality of sets of input signals based on the plurality of sets of input signals generated in step (m) by using a genetic algorithm.